REMARKS

This paper is being provided in response to the Office Action mailed September 16, 2002, for the above-referenced application. In this response, Applicants have added new claim 24 and amended claims 1, 2, 4-7, 17 and 20-23 in order to clarify that which Applicants consider to be the invention. Further, Applicants have cancelled claims 10-16. Applicants respectfully submit that the amendments to the claims and the new claim are supported by the originally-filed application.

The rejection of claims 4-7 and 20-22 under 35 U.S.C. 112, second paragraph, has been addressed by the amendments to the claims contained herein. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of Claims 1-3, 7, 9 and 17-19 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,111,448 to Shibayama (hereinafter "Shibayama") is hereby traversed and reconsideration thereof is respectfully requested in view of the amendments to the claims contained herein.

Applicants' independent claim 1, as amended herein, recites a delay locked loop (DLL) circuit comprising a delay circuit which is connected to first and second nodes and which delays an original clock signal supplied to the first node based on a delay control signal. The delay circuit generates first to n-th (n is an integer more than 1) internal clock signals. The first internal clock signal is outputted from the second node. The internal clock signals other than the first internal clock signal are outputted from the delay circuit without passing through the second

node and lead the first internal clock signal in phase by a predetermined phase value. The original clock signal is a frequency variable clock signal and the delay circuit includes a first delay section with a frequency dependent delay time and a second delay section with a fixed delay time. A phase comparing circuit compares the original clock signal and the first internal clock signal and outputs a phase difference. A delay control circuit outputs the delay control signal to the delay circuit based on the phase difference outputted from the phase comparing circuit. Claims 2-9 depend directly or indirectly on claim 1.

Applicants' independent claim 17, as amended herein, recites a method of generating timing signals, comprising delaying an original clock signal supplied to a first node based on a delay control signal. First to n-th (n is an integer more than 1) internal clock signals are generated from the delayed original clock signal. The first internal clock signal is outputted from a second node and the internal clock signals other than the first internal clock signal are outputted without passing through the second node and lead the first internal clock signal in phase by a predetermined value. The original clock signal is a frequency variable clock signal, and a first delay section with a frequency dependent delay time and a second delay section with a fixed delay time control delay of the original clock signal and the internal clock signals. A phase difference between the original clock signal and the first internal clock signal is detected. The delay control signal is generated based on the detected phase difference. Claims 18-23 depend directly or indirectly on independent claim 17.

The Shibayama reference discloses a clock signal distribution circuit for distributing a clock signal at high speed and with less phase displacement on a large scale integrated circuit.

The circuit utilizes two variable delay circuits, a clock tree, a control circuit and a phase comparison circuit.

Applicants' claims, as amended, recite the feature that an original clock signal is a frequency variable clock signal and a delay circuit for delaying the original clock signal and internal clocks signals includes a first delay section *with a frequency dependent delay time* and a second delay signal with a fixed delay time. With this feature, even if the frequency of the original clock signal is changed, the first delay section with frequency dependent delay generates a coarsely controlled clock signal and the second delay section with fixed delay generates the first internal clock signal, allowing other internal clock signals that lead the first internal clock signal in phase by a predetermined value to be generated

Shibayama discloses a variable delay circuit and clock tree; however, the variable delay circuit has *no frequency dependency in the delay time*, as shown in Figure 8 and described in col. 7, line 64 to col. 8, line 28. Therefore, when the frequency of the original clock signal is changed, it would be difficult to control the phases of the delivered clock signal. Applicants respectfully submit that Shibayama does not teach or suggest the feature of a delay circuit for delaying the original clock signal and internal clocks signals that includes a first delay section with a frequency dependent delay time and a second delay signal with a fixed delay time, as is claimed by Applicants. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claims 4-6, 8, and 20-22 under 35 U.S.C. 103(a) as being unpatentable over Shibayama is hereby traversed and reconsideration thereof is respectfully requested in view of the amendments to the claims contained herein.

Applicants' claims 4-6 and 8 depend from independent claim 1. Applicants' claims 20-22 depend from independent claim 17. For the reasons set forth above with respect to Applicants' claim 1 and claim 17, Applicants respectfully submit that Shibayama does not teach or suggest at the least the above-noted features. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Applicants have added new claim 24 and respectfully submit that it is patentable over the prior art of record.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4042.

Respectfully submitted,
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CLEAN-COPY LIST OF ALL PENDING CLAIMS AS AMENDED HEREIN

1. (Amended) A DLL (delay locked loop) circuit, comprising:

a delay circuit which is connected to first and second nodes, and which delays an original clock signal supplied to said first node based on a delay control signal and generates first to n-th (n is an integer more than 1) internal clock signals, wherein said first internal clock signal is outputted from said second node, and the internal clock signals other than said first internal clock signal are outputted from said delay circuit without passing through said second node, and lead the first internal clock signal in phase by a predetermined value, and wherein said original clock signal is a frequency variable clock signal and said delay circuit includes a first delay section with a frequency dependent delay time and a second delay section with a fixed delay time;

a phase comparing circuit which compares said original clock signal supplied from said first node and said first internal clock signal supplied from said second node, and outputs a phase difference of said original clock signal and said first internal clock signal; and

a delay control circuit which outputs said delay control signal to said delay circuit based on the phase difference outputted from said phase comparing circuit.

2. (Amended) The DLL circuit according to claim 1, wherein

said first delay section delays said original clock signal based on said delay control signal to generate a first delay signal; and

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said second delay section which is provided between said second node and said first delay section, and delays the first delay signal to generate said first to n-th internal clock signals, and outputs said first internal clock signal from said second node, and the internal clock signals other than said first internal clock signal without passing through said second node.

3. The DLL circuit according to claim 2, wherein said second delay circuit comprises:

a plurality of delay elements connected in series, and said first to n-th internal clock signals are outputted from different ones of said plurality of delay elements.

4. (Amended) The DLL circuit according to claim 3, wherein each of said plurality of delay elements delays said first delay signal by substantially a same amount of time.

5. (Amended) The DLL circuit according to claim 3, wherein each of said plurality of delay elements delays said first delay signal by an amount of time different from other delay elements.

6. (Amended) The DLL circuit according to claim 3, wherein an amount of time by which each of said plurality of delay elements delays said first delay signal is predetermined.

7. (Amended) The DLL circuit according to claim 3, wherein an amount of time by which each of said plurality of delay elements delays said first delay signal is independent of a frequency of said original clock signal.

17. (Amended) A method of generating timing signals, comprising the steps of:

(a) delaying an original clock signal supplied to a first node based on a delay control signal;

(b) generating first to n-th (n is an integer more than 1) internal clock signals from the delayed original clock signal, wherein said first internal clock signal is outputted from a second node, and the internal clock signals other than said first internal clock signal are outputted without passing through the second node, and lead said first internal clock signal in phase by a predetermined value, and wherein the original clock signal is a frequency variable clock signal, and a first delay section with a frequency dependent delay time and a second delay section with a fixed delay time control delay of the original clock signal and the internal clock signals;

(c) detecting a phase difference between said original clock signal and said first internal clock signal; and

(d) generating said delay control signal based on the detected phase difference.

18. The method according to claim 17, wherein the (a) delaying step comprises the steps of:

(e) delaying said original clock signal based on said delay control signal to generate a first delay signal; and

(f) delaying the first delay signal to generate said first to n-th internal clock signals.

19. The method according to claim 18, wherein the (f) delaying step comprises the step of:

(g) delaying the first delay signal by a plurality of delay elements connected in series, wherein said first to n-th internal clock signals are outputted from different ones of said plurality of delay elements.

20. (Amended) The method according to claim 19, wherein each of said plurality of delay elements delays said first delay signal by substantially a same amount of time.

21. (Amended) The method according to claim 19, wherein each of said plurality of delay elements delays said first delay signal by an amount of time different from other delay elements.

22. (Amended) The method according to claim 19, wherein an amount of time by which each of said plurality of delay elements delays said first delay signal is predetermined.

23. (Amended) The method according to claim 19, wherein an amount of time by which each of said plurality of delay elements delays said first delay signal is independent of a frequency of said original clock signal.

24. (New Claim) A synchronous memory, comprising:

a delay locked loop circuit that delays an original clock signal supplied as an input, said delay locked loop circuit producing as an output a plurality of internal clock signals, a first of said plurality of internal clock signals being said original clock signal delayed by a first quantity and a second of said plurality of internal clock signals being said original clock signal delayed by a second quantity different than said first quantity, said delay locked loop circuit comprising:

a variable delay section with a frequency dependent delay time that delays said original clock signal generated as a first delay signal based on a phase difference between said original clock signal and one of said plurality of internal clock signals; and

a fixed delay section that is a multi-stage structure of delay elements that delays said first delay signal by a predetermined amount, said second internal clock signal being generated as an output of one of said stages;

a logic circuit that generates an enable signal in synchronism with said second internal clock signal and a latch signal in synchronism with said first internal clock signal; and

a memory section that performs one of a read and write operation of data in response to said enable signal and latches said data for one of input and output to said memory section in response to said latch signal.